REMARKS

Claim 1 incorporates the subject matter of dependent claims 5 and 7, and claim 8 incorporates the subject matter of dependent claims 12 and 14. Entry of this amendment, reconsideration, and allowance of the subject application are respectfully requested.

The Examiner admits that Gold does not disclose that the mapping circuit is an interface circuit operable to adapt values and timings of signals passed between the self-test controller and the at least one memory to accommodate differing value and timing properties of the at least one memory. The Examiner also concedes that Gold does not disclose a plurality of memories, each having an associated mapping circuit. Hence, independent claims 1 and 8 are novel with regard to Gold.

The Examiner argues that since Gold discloses the address converter can be adapted to support built-in self-repair of the embedded memory array, Gold "implicitly" teaches that the address mapper includes circuitry to synchronize the timing of signals connected to the memory array. This argument is impermissible hindsight.

Gold relates to address remapping to enable self-testing of a particular embedded memory in a particular electronic device. Gold teaches that the remapping is required due to a difference between a logical mapping and a physical mapping of a given memory that arises due to the memory circuitry having been adapted to reduce memory cell access delay by evenly distributing the load on each row address wire or row address pre-decode wire across its length. Because a self-test controller generates physical addresses, an address remapper is required to convert the physical addresses to logical

addresses due to the fact that, for the particular memory, the logical mapping differs from the physical mapping (see Gold paragraphs 5 and 7). Gold neither discloses nor suggests that the address remapper could be used to facilitate re-use of the self-test controller with a number of different memories having different mappings between physical memory locations and the logical addresses between these locations as in the present application (see, e.g., the description at page 3, lines 12-24).

Indeed, there is no hint that Gold's self-test controller could be used with any memory other than the particular embedded memory with which it is associated. Because Gold's self-test controller is dedicated to testing one particular memory, the self-test controller is specifically designed so that its signal timings and values are consistent with the signal timings and values specifically required for the particular embedded memory.

But even if Gold's address converter could be adapted to support built-in self-repair of the embedded memory array, Gold does not teach how the address converter could be adapted to perform this function. Nor would a person of ordinary skill in the art consider that "self-repair" functionality would involve synchronization of signals and values between the self-test controller and the memory array. Indeed, to reliably repair the memory circuit, the repair would have to be effective when the memory was not in self-test mode so that the synchronization between the self-test controller and the memory would be relevant to the test mode only and not the operational mode. Thus, the Examiner's reasoning that self-repair "implicitly" discloses synchronization between self-test controller and memory is not plausible and cannot reasonably be maintained.

The Examiner contends in paragraph 10 of the Office action that since Gold discloses an address remapper for use with a single memory and since Gold discloses that the electronic device comprising the memory includes more than one data bus, that it would have been obvious to the skilled person to modify the electronic device to comprise a plurality of memories and a plurality of memory address converter circuits. But Gold's paragraph 2 simply describes that the electronic apparatus could comprise a read bus as well as a write bus. That paragraph does not teach more than one embedded memory, and it certainly does not suggest a mapping circuit provided for each of a plurality of memories. Because Gold neither discloses nor suggests that the mapping circuit serves the function of enabling a generic self-test controller to be adapted for use with a plurality of different memories, each having different logical-to-physical address mappings, a person of ordinary skill in the art would not have been motivated to adapt Gold's system to incorporate further memories, each having an associated mapping circuit.

Claim 1 recites a plurality of memories, each having an associated mapping circuit, and specifies that the mapping circuit is part of an interface circuit operable to adapt signal values and timings passed between the self-test controller and the respective memories to accommodate the particular value and timing properties of the respective memory. The combination of the plurality of memories and the signal value and timing interfacing provided by the mapping circuit enables the claimed self-test controller to be re-usable with a plurality of different memories. Concentrated customization needed for

the different memories in an interface circuit significantly benefits from this self-test controller reuse.

Gold does not disclose a plurality of memories having associated mapping circuits. Furthermore, Gold fails to teach--explicitly or implicitly--mapping circuits operable to adapt signal timings and values as specified in claims 1 and 8. Gold also fails to provide the skilled person with any motivation to provide a generic self-test controller that is re-usable with a plurality of different memories. Absent Applicant's teachings, there is no basis to modify Gold's single memory dedicated device into the claimed multiple memory adaptable device.

The application is in condition for allowance. An early notice to that effect is earnestly solicited

Respectfully submitted,

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